18/5/2 (Item 2 from file: 350)
DIALOG(R)File 350: Derwent WPIX

0014266406 *Drawing available*
WPI Acc no: 2004-452766/200443
XRPX Acc No: N2004-358449
Audiovisual domestic digital bus heterogeneous network destination node information synchronization having input node second synchronization packet set following first packet and inserting synchronization mark second packet
Patent Assignee: CANON KK (CANO)
Inventor: BERNIER C; EL KOLLI Y; EL KOLLY Y S; KOLLI Y E

Patent Family (3 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
FR 2848056	A1	20040604	FR 200214989	A	20021128	200443	B
US 20040246995	A1	20041209	US 2003717455	A	20031121	200481	E
US 7500019	B2	20090303	US 2003717455	A	20031121	200917	E

Priority Applications (no., kind, date): FR 200214989 A 20021128

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
FR 2848056	A1	FR	46	9	

Alerting Abstract FR A1
NOVELTY - The node information synchronization technique has a sub network passing **first packets** and a base network sending **second packets**. When there is a determined event, the input node forms a **second** synchronization **packet** so that the synchronization corresponds to the useful information of the **first packet**. A **synchronization mark** is inserted in the **second** synchronization **packet**.
USE - Audiovisual digital bus heterogeneous network destination node information synchronization.
ADVANTAGE - Does not need prior initialization of the receiver terminal and is simple and low cost.
DESCRIPTION OF DRAWINGS - The figure shows a schematic of a heterogeneous audiovisual network which uses the synchronization process

18/5/10 (Item 10 from file: 350)
DIALOG(R)File 350: Derwent WPIX

0009392764 *Drawing available*
WPI Acc no: 1999-328457/**199928**
XRPX Acc No: N1999-246369
Method of evaluating a digital data flow using packet data communications with synchronization bits in each data packet and defined identifier bit positions
Patent Assignee: GRUNDIG AG (GRUG)
Inventor: HORN B

Patent Family (2 patents, 25 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
DE 19820936	C1	19990602	DE 19820936	A	19980509	199928	B
EP 957640	A2	19991117	EP 1999108992	A	19990506	199953	E

Priority Applications (no., kind, date): DE 19820936 A 19980509

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
DE 19820936	C1	DE	6	1	
EP 957640	A2	DE			
Regional Designated States,Original	AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				

Alerting Abstract DE C1
NOVELTY - the method involves separating (3) the identifying bits from the defined positions of the **first packet**, storing them temporarily and comparing with similarly obtained bits from a **subsequent packet**. If they coincide a further packet's bits are extracted and compared with the stored bits. If a lack of coincidence is detected an indication signal is generated
DESCRIPTION - An INDEPENDENT CLAIM is also included for an arrangement for implementing the method
USE - for evaluating a digital data flow using packet data communications with **synchronization bits** in each data packet and defined identifier bit positions
ADVANTAGE - enables rapid and reliable detection of changes in the data flow, esp. in information transferred in addition to video and audio data
DESCRIPTION OF DRAWINGS - the drawing shows a block diagram of an associated arrangement
1 synchronous byte detector
2 control unit
3 identity bit separator
6 data separator

18/5/12 (Item 12 from file: 350)
DIALOG(R)File 350: Derwent WPIX

0008831116 *Drawing available*
WPI Acc no: 1998-377059/**199832**
XRPX Acc No: N1998-294882
Packet stream modification method for synchronous bit insertion in MPEG of digital TV signal communication system - involves concatenating first substitute sync byte with second substitute sync byte which are then interleaved in desired bit position of packet stream
Patent Assignee: GEN INSTR CORP DELAWARE (GENN)
Inventor: MORONEY P; SCHMIDT M S

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5771239	A	19980623	US 1995560008	A	19951117	199832	B

Priority Applications (no., kind, date): US 1995560008 A 19951117

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 5771239	A	EN	17	7	

Alerting Abstract US A
The method involves replacing the conventional sync byte in the **first packet** of a packet stream by a first substitute sync byte. The conventional sync byte in the **second packet** of the packet stream is deleted, thereby another byte is replaced to the deleted sync byte position.
Then the second substitute sync byte is moved into the bit position from where the bit is moved to the deleted sync byte position. Then the first sync byte is concatenated with the second sub-byte which are then interleaved in the desired byte position of the **first** and **second packets**.
ADVANTAGE - Avoids error generation in packet transmission system. Enables modification of transport packets at different packet size.

0008769526 *Drawing available*
WPI Acc no: 1998-312839/**199827**
XRPX Acc No: N1998-245188
Image data transmission method - converting 8-bit word-string data into 10-bit word-string data with either negative running disparity or positive running disparity depending on previous disparity
Patent Assignee: SONY CORP (SONY)
Inventor: YAMASHITA S

Patent Family (4 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 1998023060	A1	19980528	WO 1997JP4263	A	19971121	199827	B
JP 10523484	X	19990406	WO 1997JP4263	A	19971121	199924	E
			JP 1998523484	A	19971121		
US 6054944	A	20000425	WO 1997JP4263	A	19971121	200027	E
			US 1998120852	A	19980722		
US 6323787	B1	20011127	WO 1997JP4263	A	19971121	200175	E
			US 1998120852	A	19980722		
			US 2000558011	A	20000425		

Priority Applications (no., kind, date): JP 1996312276 A 19961122

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 1998023060	A1	JA	38	10		
National Designated States,Original	JP US					
JP 10523484	X	JA			PCT Application	WO 1997JP4263
					Based on OPI patent	WO 1998023060
US 6054944	A	EN			Continuation of application	WO 1997JP4263
US 6323787	B1	EN			Continuation of application	WO 1997JP4263
					Continuation of application	US 1998120852
					Continuation of patent	US 6054944

Alerting Abstract WO A1
The method involves transmitting 8-bit word-string data indicating signal information by converting the data into 10-bit word-string data containing word **synchronising** data. The 8-**bit** word-string data indicting the signal information are obtained, and the data are converted into the 10-bit word-string data by performing 8-10 bit conversion after inserting 8-**bit synchronising** data. 8-**bit** auxiliary word data are converted into 10-bit neutral word data two by two in response to a specified timing signal.
At the time of performing the 8-10 bit conversion, the 8-**bit** word **synchronising** data are converted into 10-**bit** word **synchronising** data with a negative running disparity when the immediately prior word data has a positive running disparity. The 8- **bit** word **synchronising** data are converted into 10-**bit** word **synchronising** data having a positive running disparity when the immediately prior word data has a negative running disparity.

ADVANTAGE - Allows obtaining required signal synchronising state when signal information is reproduced on reception side.

0007442510 *Drawing available*
WPI Acc no: 1996-051680/**199606**
Related WPI Acc No: 2001-140132
XRPX Acc No: N1996-043319

Audio and video digital signal transmission method e.g. for TV, VTR - assembling data packet containing audio and video data and start and end synchronisation codes with auxiliary data indicating data type and volume

Patent Assignee: SONY CORP (SONY)
Inventor: FUJISAKI N

Patent Family (9 patents, 5 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 690630	A2	19960103	EP 1995304486	A	19950626	199606	B
JP 8018914	A	19960119	JP 1994144403	A	19940627	199613	E
US 5903569	A	19990511	US 1995493732	A	19950622	199926	E
US 6272149	B1	20010807	US 1995493732	A	19950622	200147	E
			US 1997879116	A	19970619		
			US 2000532719	A	20000322		
JP 3329076	B2	20020930	JP 1994144403	A	19940627	200271	E
US 6493357	B1	20021210	US 1995493732	A	19950622	200301	E
			US 1997879116	A	19970619		
			US 2000532753	A	20000322		
EP 690630	B1	20040519	EP 1995304486	A	19950626	200433	E
			EP 2000203551	A	19950626		
DE 69533050	E	20040624	DE 69533050	A	19950626	200442	E
			EP 1995304486	A	19950626		
DE 69533050	T2	20050602	DE 69533050	A	19950626	200537	E
			EP 1995304486	A	19950626		

Priority Applications (no., kind, date): JP 1994144403 A 19940627

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 690630	A2	EN	26	15		
Regional Designated States,Original	DE FR GB NL					
JP 8018914	A	JA	15			
US 6272149	B1	EN			Continuation of application	US 1995493732
					Continuation of application	US 1997879116
					Continuation of patent	US 5903569
JP 3329076	B2	JA	15		Previously issued patent	JP 08018914
US 6493357	B1	EN			Division of application	US 1995493732

					Continuation of application	US 1997879116
					Division of patent	US 5903569
EP 690630	B1	EN			Related to application	EP 2000203551
					Related to patent	EP 1069780
Regional Designated States,Original	DE FR GB NL					
DE 69533050	E	DE			Application	EP 1995304486
					Based on OPI patent	EP 690630
DE 69533050	T2	DE			Application	EP 1995304486
					Based on OPI patent	EP 690630

Alerting Abstract EP A2

The method involves assembling a data packet portion (1440) containing video and audio data, a start synchronisation code and an end **synchronisation** code for **bit synchronisation**. An auxiliary data portion (268) is located between the start and end synchronisation codes.

The auxiliary data portion consists of an area indicating the data type and a byte count indicating data volume and a second data portion. A line number of data is provided at the leading end of the auxiliary data portion. The data packet is transmitted via a communications network e.g. LAN.

USE/ADVANTAGE - E.g. digital serial data interface. Optional number of line numbers can be set. Allows asymmetrical transmission e.g. 1:n. Efficient and economical as easily extendible with low maintenance required.

0012461244 *Drawing available*
WPI Acc no: 2002-407315/200244
XRPX Acc No: N2002-319885

Synchronization control device for audio communication system, produces synchronization point information on inserting predetermined number of zero data between two successive leading data packets

Patent Assignee: TOSHITANI M (TOSH-I); YAMAHA CORP (NIHG)
Inventor: TOSHITANI M; TOSHITANI T

Patent Family (8 patents, 28 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 1189140	A1	20020320	EP 2001121459	A	20010907	200244	B
JP 2002084264	A	20020322	JP 2000273279	A	20000908	200244	E
US 20030063627	A1	20030403	US 2001969522	A	20011002	200331	NCE
JP 3417392	B2	20030616	JP 2000273279	A	20000908	200340	E
EP 1189140	B1	20060208	EP 2001121459	A	20010907	200612	E
DE 60117078	E	20060420	DE 60117078	A	20010907	200628	E
			EP 2001121459	A	20010907		
US 7042911	B2	20060509	US 2001969522	A	20011002	200632	NCE
DE 60117078	T2	20060914	DE 60117078	A	20010907	200663	E
			EP 2001121459	A	20010907		

Priority Applications (no., kind, date): JP 2000273279 A 20000908; EP 2001121459 A 20010907; US 2001969522 A 20011002

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 1189140	A1	EN	20	9		
Regional Designated States,Original	AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2002084264	A	JA	13			
JP 3417392	B2	JA	12		Previously issued patent	JP 2002084264
EP 1189140	B1	EN				
Regional Designated States,Original	DE FR GB					
DE 60117078	E	DE			Application	EP 2001121459
					Based on OPI patent	EP 1189140
DE 60117078	T2	DE			Application	EP 2001121459
					Based on OPI patent	EP 1189140

Alerting Abstract EP A1

NOVELTY - A **synchronization** point controller (205) detects leading data packets sequentially output from FIFO buffer (23). If the time period between two detected successive leading data packets is below the period of **synchronized** frame, a predetermined number of zero data are inserted between two detected successive leading data packets and **synchronization** point information is output to a **synchronism** evaluation unit (204).

USE - For receiving isochronously transferred packet data from USB, in audio communication system.

ADVANTAGE - Prevents erroneous determination regarding an underflow or overflow in FIFO buffer. Permits appropriate **synchronized** reproduction of received data without adverse effects on **synchronism** evaluation.

DESCRIPTION OF DRAWINGS - The figure shows the block diagram of **synchronization** control device.

23 FIFO buffer

204 **Synchronism** evaluation unit

205 **Synchronization** point controller

NPL

[related to your application?]

15/5/2 (Item 1 from file: 23)
DIALOG(R)File 23: CSA Technology Research Database

0011806289 IP Accession No: 200904-71-0953681; 200904-61-0967991; 20090940471; A09-99-0942186
Methods for the insertion and processing of information for the synchronization of a destination node with a data stream crossing a basic network of heterogeneous network, and corresponding nodes

Kolli, Yacine El; Bernier, Cyril
, USA
Publisher Url: http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u =/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=75 00019.PN.&OS=pn/7500019&RS=PN/7500019

Document Type: Patent
Record Type: Abstract
Language: English
File Segment: Metadex; Mechanical & Transportation Engineering Abstracts; ANTE: Abstracts in New Technologies and Engineering; Aerospace & High Technology

Abstract:
In a method for the insertion of information to synchronize a destination node with a data stream transmitted from an entry terminal in a heterogeneous network, the heterogeneous network includes at least one sub-network conveying **first packets** and one basic network conveying **second packets**. The entry terminal is connected to the sub-network. The sub-network is connected to the basic network by means of an entry terminal forming the **second packets** from at least one sub-part of at least one **first packet**. At the occurrence of at least one pre-determined event, the entry node: forms a **second** synchronization **packet** such that the beginning of the useful information of the **second** synchronization **packet** corresponds to the beginning of a **first packet**; inserts a synchronization marker in the **second synchronization packet**; and modifies the size of a **second packet** preceding the **second** synchronization **packet**.

Descriptors: Synchronization; Networks; Synchronism; Terminals; Insertion; Streams; Conveying; Markers; Inserts; Forming
Subj Catg: 71, General and Nonclassified; 61, Design Principles; 99, General

0015168174 **E.I. COMPENDEX No:** 2002357065500
New protocol transfer module for USB2.0 -to- IEEE 1394 interfaces using synchronous packet control for audio and video data streams

Fujimori, Shingo; Sakurai, Toshimi; Ikenoya, Kazuyuki; Shinmura, Satoshi; Asada, Hideyuki
Conference Title: 2002 Digest of Technical Papers
Conference Location: Atlanta,GA United States **Conference Date:** 20020618-20020620
Sponsor: IEEE
E.I. Conference No.: 59498
Digest of Technical Papers - IEEE International Conference on Consumer Electronics (Dig Tech Pap IEEE Int Conf Consum Electron) (United States) 2002 , IEEE 02ch37300 (314-316)
Publication Date: 20020903
Publisher: Institute of Electrical and Electronics Engineers Inc.
CODEN: DTPEE **ISSN:** 0747-668X
Document Type: Conference Paper; Conference Proceeding **Record Type:** Abstract
Treatment: T; (Theoretical)
Language: English **Summary Language:** English
Number of References: 6
This paper describes the development of a protocol transfer module for universal serial bus interface version 2.0 (USB2.0)[6] -to- IEEE 139411] interface using synchronous packet control for audio and video (AV) data streams. This protocol transfer module can easily transmit AV data streams from a personal computer (PC) embedded an USB2.0 interface port to a digital video camcorder (DVC) unless the AV data stream unsynchronizing between the USB2.0 and IEEE 1394 interfaces. This protocol transfer module is used for transmitting and editing AV data streams on PC's and AV consumer appliances standardized with IEEE 1394. USB2.0 and IEEE 1394 interfaces are largely used for consumer electronics appliances especially Home Network devices. This protocol transfer module is used for AV consumer appliances standardized with IEEE 1394[2][3][4][5]. Most of users having PC's embedded either USB1.1 or USB2.0 interface port could not receive and edit AV data streams obtained from a DVC standardized with IEEE 1394. Because there is nothing to bridge the AV data streams between the USB2.0 and IEEE 1394 interfaces now.
Descriptors: Consumer electronics; Domestic appliances; Interfaces (computer); Network protocols; Personal computers; Printed circuit boards; *Packet networks
Identifiers: Video data streams
Classification Codes:
722.4 (Digital Computers & Systems)
722.2 (Computer Peripheral Equipment)
714.2 (Semiconductor Devices & Integrated Circuits)
723 (Computer Software, Data Handling & Applications)
716 (Electronic Equipment, Radar, Radio & Television)
715 (Electronic Equipment, General Purpose & Industrial)
522 (Gas Fuels)

27/5/3 (Item 2 from file: 2)
DIALOG(R)File 2: INSPEC

07018561
Title: Realisation and performance of IEEE 1355 DS and HS link based, high speed, low latency packet switching networks
Author(s): Zhu, M.; Thornley, D.A.; Pech, J.; Martin, B.; Madsen, N.H.; Heeley, R.; Haas, S.; Dobinson, R.W.; Anderson, C.R.
Author Affiliation: CERN, Geneva, Switzerland
Journal: IEEE Transactions on Nuclear Science , vol.45 , no.4 , pp.1849-53
Publisher: IEEE
Country of Publication: USA
Publication Date: Aug. 1998
Conference Title: Tenth Conference on Real-Time (RT'97)
Conference Date: 22-26 Sept. 1997
Conference Location: Beaune, France
ISSN: 0018-9499
SICI: 0018-9499(199808)45:4:1L.1849:RPI1;1-U
CODEN: IETNAE
U.S. Copyright Clearance Center Code: 0018-9499/98/$10.00
Item Identifier (DOI): 10.1109/23.710949
Language: English
Document Type: Conference Paper in Journal (PA)
Treatment: Practical (P); Experimental (X)
Abstract: We report on the construction of a 1024 node switching network using IEEE 1355 DS link technology. The nodes are interconnected by a switching fabric based on the STC104 packet switch. The system has been designed and constructed in a modular way in order to allow a variety of different network topologies to be investigated. Network throughput and latency have been studied for different topologies under various traffic conditions including those expected within the second level trigger of the ATLAS experiment. Initial experience using 1 Gbaud IEEE 1355 HS links and switches is also presented (*16 refs.*)
Subfile(s): A (Physics); B (Electrical & Electronic Engineering); C (Computing & Control Engineering)
Descriptors: high energy physics instrumentation computing; IEEE standards; network topology; packet switching; telecommunication network routing; telecommunication standards
Identifiers: 1024 node; packet switching networks; low latency; IEEE **1355** DS link; STC104 **packet** switch; modular; throughput; latency; second level trigger; ATLAS; IEEE 1355 HS link; data strobe; high speed link
Classification Codes: A2980C (Computer systems for nuclear information processing); B6150C (Communication switching); B7420 (Particle and radiation detection and measurement); B6150P (Communication network design, planning and routing); C7320 (Physics and chemistry computing)
INSPEC Update Issue: 1998-036

27/5/4 (Item 3 from file: 2)
DIALOG(R)File 2: INSPEC

06963894
Title: **The Macrame 1024 node switching network**
Author(s): Haas, S.; Thornley, D.A.; Zhu, M.; Dobinson, R.W.; Martin, B.
Author Affiliation: CERN, Geneva, Switzerland
Journal: Microprocessors and Microsystems , vol.21 , no.7-8 , pp.511-18
Publisher: Elsevier
Country of Publication: UK
Publication Date: 30 March 1998
ISSN: 0141-9331
SICI: 0141-9331(19980330)21:7/8L.511:M1NS;1-Y
CODEN: MIMID5
Document Number: S0141-9331(98)00044-1
U.S. Copyright Clearance Center Code: 0141-9331/98/$19.00
Language: English
Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: We report on the construction of a large network testbed using IEEE 1355 DS-link technology. One thousand nodes are interconnected by a switching fabric based on the STC104 packet switch. The system has been designed and constructed in a modular way in order to allow a variety of different network topologies to be investigated. Network throughput and latency have been studied for different network topologies under various traffic conditions (*12 refs.*)
Subfile(s): B (Electrical & Electronic Engineering); C (Computing & Control Engineering)
Descriptors: computer networks; multiprocessor interconnection networks; network topology
Identifiers: network testbed; IEEE **1355**; switching fabric; STC104 **packet** switch; network topologies; throughput; latency; traffic conditions; Macrame
Classification Codes: B6210L (Computer communications); B1110 (Network topology); C4230M (Multiprocessor interconnection); C5220P (Parallel architecture); C5620 (Computer networks and techniques)
INSPEC Update Issue: 1998-027

0011795021 IP Accession No: 200904-71-0782813; 200904-61-0797219; 20090770927; A09-99-0772782

Method of generating timestamps for isochronous data

Stallkamp, Richard Wissler
, USA

Publisher Url: http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u =/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=74 96098.PN.&OS=pn/7496098&RS=PN/7496098

Document Type: Patent
Record Type: Abstract
Language: English
File Segment: Metadex; Mechanical & Transportation Engineering Abstracts; ANTE: Abstracts in New Technologies and Engineering; Aerospace & High Technology

Abstract:
A method of generating timestamps for isochronous data includes locking a data stream time and an isochronous network time to a local clock signal such that a bi-directional mapping may be made between the two time domains. Timing information is extracted from both IEEE **1394** based data **packets** and a conventional house reference signal in order to obtain scale and offset factors that exist between the two signals. The scale and offset factors are applied to a generated video clock signal in order to predict a future video time in terms of IEEE 1394 time.

Descriptors: Clocks; Offsets; Reference signals; Streams; Time measurements; Networks; Locking; Mapping; Time domain; Houses
Subj Catg: 71, General and Nonclassified; 61, Design Principles; 99, General

0015287622 **E.I. COMPENDEX No:** 2002477229731

Packet scheduling for WDM fiber delay line buffers in photonic packet switches

Yamaguchi, Takashi; Baba, Ken-Ichi; Murata, Masayuki; Kitayama, Ken-Ichi
Corresp. Author/Affil: Yamaguchi, T.: Dept. of Informatics and Math. Sci., Osaka University, 1-3 Machikaneyama, Toyonaka, Osaka 560-8531, Japan
Corresp. Author email: t-yamagt@ics.es.osaka-u.ac.jp
Editor(s): Ghani, N.; Sivalingam, K.M.
Conference Title: OptiComm 2002 Optical Networking and Communications
Conference Location: Boston, MA United States **Conference Date:** 20020730-20020731
Sponsor: SPIE
E.I. Conference No.: 60241
Proceedings of SPIE - The International Society for Optical Engineering (Proc SPIE Int Soc Opt Eng) (United States) 2002 4874/- (262-273)
Publication Date: 20021126
Publisher: SPIE
CODEN: PSISD **ISSN:** 0277-786X
Item Identifier (DOI): 10.1117/12.475303
Document Type: Conference Paper; Conference Proceeding **Record Type:** Abstract
Treatment: T; (Theoretical)
Language: English **Summary Language:** English
Number of References: 13

In this paper, we comparatively evaluate **two** photonic **packet** switch architectures with WDM-FDL buffers for **synchronized** variable length packets. The first one is an output buffer type switch, which stores packets in the FDL buffer attached to each output port. Another is a shared buffer type switch, which stores packets in the shared FDL buffer. The performance of a switch is greatly influenced by its architecture and the packet scheduling algorithm. We compare the performance of these two packet switches by applying different packet scheduling algorithms. Through simulation experiments, we show that each architecture has a parameter region for achieving a better performance. For the shared buffer type switch, we found that void space introduces unacceptable performance degradation when the traffic load is high. Accordingly, we propose a void space reduction method. Our simulation results show that our proposed method enables to the shared buffer type switch to outperform the output buffer type switch even under high traffic load conditions.

Descriptors: Algorithms; Packet switching; Photons; Scheduling; Wavelength division multiplexing; *Optical communication
Identifiers: Photonic packet switches
Classification Codes:
717.1 (Optical Communication Systems)
741.1 (Light & Optics)
716 (Electronic Equipment, Radar, Radio & Television)
723 (Computer Software, Data Handling & Applications)